Dr. Amrita Kumari

Ph.D. (Electronics Engineering)
Indian Institute of Technology (Indian School of Mines), Dhanbad

Email: kamrita2610@gmail.com, amrita_elex@yahoo.com
Contact numbers: +91 8077729396, +91 9939708036

Address:

ETH-265, Sector-2,
BHEL, Ranipur,
Haridwar-249403
Uttarakhand, India

Academic Qualifications:

Sl. No.	Degree	Year	University	Subject	CGPA
1.	Ph.D. (Electronics)	2017	Indian Institute of Technology (Indian School of Mines) Dhanbad	Thesis title: "Computational techniques and performance evaluation of nanoscale strained MOSFETs and related CMOS circuits"	-
2.	M.E. (VLSI Design)	2012	Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)	VLSI Design	8.97
3.	B.E. (Electronics & Telecommun-ication)	2009	Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.)	Electronics and Telecommunication Engineering	8.48

Professional Experience:

Position Held	Name of Institute	Duration

Assistant Professor	Dept. of Electronics & Telecommunication Engineering, Shri Shankaracharya Group of Institutions, Bhilai	2010-2012
R&D Engineer	Abhitech Energycon Ltd.	Jan. 2017- Aug. 2022
Assistant Professor	Quantum University, Roorkee	Oct. 2022-present

Laboratories conducted:

1. VLSI Design (B.Tech + M.Tech)
2. Basic Electronics

Software Technical Skills:

1. Xilinx
2. Microwind
3. Tanner
4. Silvaco-TCAD
5. LASI

Publications:

International Journals:

1. **A. Kumari,** S. Kumar, T. K. Sharma and M. K. Das, "On the C-V characteristics of nanoscale strained gate-all-around Si/SiGe MOSFETs," ***Solid State Electronics***, vol. 154, pp. 36–42, Apr. 2019. (**Impact Factor-1.99**)
2. S. Kumar, **A. Kumari,** and M. K. Das, "Modeling gate-all-around Si/SiGe MOSFETs and circuits for digital applications," ***Journal of Computational Electronics***, vol. 16, no. 1, pp. 47–60, Jan. 2017. (**Impact Factor-1.807**)
3. S. Kumar, **A. Kumari,** and M. K. Das, "Strain induced changes in the performance of strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ MOSFETs and circuits for digital applications," ***Journal of Central South University***, vol. 24, no. 6, pp. 1233-1244, Jun. 2017. (**Impact Factor- 1.716**)
4. S. Kumar, **A. Kumari,** and M. K. Das, "Development of a simulator for analyzing some performance parameters of nanoscale strained silicon MOSFET-based CMOS inverters," ***Microelectronics Journal***, vol. 55,

pp. 8–18, Sept. 2016. (**Impact Factor-1.605**)

5. A. Kumar, V. Kumar and **A. Kumari**, "An Ensemble based IDS for Edge Computing network", Inderscience Publishers (IJITCA), **Accepted**

International/National Conferences:

1. **A. Kumari**, J. Saha, A. Saini and A. Kumar, "Development of an Analytical Model of Drain Current for Junctionless GAA MOSFET including Source/Drain Resistance", ADSSS 2023, Springer.
2. **A. Kumari**, A. Saini, A. Kumar, V. Kumar and M. Kumar, "Recent Developments and Challenges in Strained Junctionless MOSFETs: A Review", in *Proc. **IEEE** CISES-2023*, Apr. 2023.
3. A. Saini, R. Kumar, **A. Kumari**, S. Kumar and M. Kumar, "Exploratory Testing of Software Product Lines using Distance Metrics", in *Proc. **IEEE** CISES-2023*, Apr. 2023.
4. A. Saini, S. Kumar, **A. Kumari**, S. Kumar, A. Kumar and A. Kumar, "An Energy-efficient Ferry-based Routing Algorithm for Scattered FANET Networks", in *Proc. **IEEE** CISES-2023*, Apr. 2023.
5. A. Kumar, S. Kumar, V. Kumar, **A. Kumari**, A. Saini, and S. Gupta, "Edge Computing based IDS Detecting Threats using Machine Learning and PyCaret: A Review", in *Proc. **IEEE** CISES-2023*, Apr. 2023.
6. A. Kumar, P. Joshi, A. Saini, **A. Kumari**, C. Chaudhary, and K. Joshi, "Smart Chatbot for Guidance About Children's Legal Rights", in *Emerging Trends in Expert Applications and Security*, V. S. Rathore et al. (eds.), Springer Nature Singapore Pte Ltd. 2023, pp. 405-412.
7. **A. Kumari** and A. Saini, "Automated Risk Analysis and Management System with IoT Integration", in Proc. *International Conf. on Multidisciplinary Research in Current Area*, Mar. 2023.
8. **A. Kumari**, A. Saini, and A. Kumar, "Modeling and analysis of junctionless gate-all-around MOSFETs", in 17th *Uttarakhand State Science & Technology Congress*, Feb. 2023.
9. **A. Kumari**, A. Saini, A. Lama, and A. Kumar, "Strained Junctionless MOSFET-A brief Review", in *Proc. **IEEE** ICFIRTP-2022*, IEEE Xplore, pp. 193-196, Nov. 2022.
10. A. Saini, R. Kumar, **A. Kumari**, and S. Kumar, "A Proposed Method of Machine Learning based Framework for Software Product Line Testing", in *Proc. **IEEE** ICFIRTP-2022*, IEEE Xplore, pp. 10-13, Nov. 2022.
11. A. Kumar, Vivek Kumar, A. Saini, **A. Kumari**, and Vipin Kumar, "Classification of Minority Attacks using Machine Learning", in *Proc. **IEEE** ICFIRTP-2022*, IEEE Xplore, pp. 101-105, Nov. 2022.
12. R. Devi, A. Kumar, V. Kumar, A. Saini, **A. Kumari**, and Vipin Kumar, "A review paper on IDS in edge computing or EoT", in *Proc. **IEEE** ICFIRTP-2022*, pp. 30-35, IEEE Xplore, Nov. 2022.

13. S. Kumar, A. Saika, **A. Kumari**, T. Sharma, and P Chauhan, "Performance evaluation of carbon-based interconnects in presence of non-conventional FET drivers" in Proc. *International Union of Materials Research Societies-The 15th International Conference on Advanced Materials*.
14. A. Nandi, S. Jha, and **A. Kumari**, "Effect of some device parameters on the transient characteristics of nanoscale CMOS inverters," in *Proc. **IEEE** International Conference on Devices, Circuits and Communication* (*ICDCCom-14*), Sept. 2014, pp. 1–6.
15. **A. Kumari** and S. Kumar, "Analysis of nanoscale strained-Si/SiGe MOSFETs including source/drain series resistance through a multi-iterative technique," in *Proc. **IEEE** 27th International Conference on VLSI Design and 13th International Conference on Embedded Systems*, Jan. 2014, pp. 427–432.
16. J. Saha, **A. Kumari**, S. Jha, and S. Kumar, "On the voltage transfer characteristics (VTC) of some nanoscale metal-oxide-semiconductor field-effect-transistors (MOSFETs)," in *Physics of Semiconductor Devices*, V.K. Jain and A. Verma, Eds. New York, NY, USA: **Springer-Verlag**, 2014,pp. 211–214.
17. **A. Kumari** and S. Kumar, "Impact of some important parameters on the drain current and threshold voltage of nanoscale strained-Si MOSFETs,"in *Proc. National Conference on Electronics, Communication and Signal Processing*, Sept. 2013, pp. 38–43.
18. P. Vaishnav, **A. Kumari**, and T. Kumar, "Integrated 32nm technology," in *Proc. National Conference on "VLSI Embedded Systems, Signal Processing and Communication Technologies*", Mar. 2010, pp. 16-17.
19. **A. Kumari** and P. Vaishnav, "Effect of 32nm scale," in *2010 National Conference "Technologia'10"*, Feb. 2010.

Papers Presented:

1. A. Kumari, A. Saini, A. Kumar, V. Kumar and M. Kumar, "Recent Developments and Challenges in Strained Junctionless MOSFETs: A Review", in Proc. IEEE CISES-2023, Apr. 2023.
2. A. Kumari and A. Saini, "Automated risk analysis and management system with IoT integration", in *International Conference on Multidisciplinary Research in Current Era*, organized by Research Solutions Global in association with Department of Psychology, Muralidhar Girls' College, Kolkata, Mar. 2023.
3. A. Kumari, A. Saini, and A. Kumar, "Modeling and analysis of junctionless gate-all-around MOSFETs", in 17th *Uttarakhand State Science & Technology Congress*, Feb. 2023.
4. A. Kumari, A. Saini, A. Lama, and A. Kumar, "Strained Junctionless MOSFET-A brief Review", in Proc. IEEE ICFIRTP-2022, IEEE Xplore, pp. 193-196, Nov. 2022.
5. A. Nandi, S. Jha, and A. Kumari, "Effect of some device parameters on the

transient characteristics of nanoscale CMOS inverters," in Proc. IEEE International Conference on Devices, Circuits and Communication (ICDCCom-14), Sept. 2014, pp. 1–6.

6. A. Kumari and S. Kumar, "Analysis of nanoscale strained-Si/SiGe MOSFETs including source/drain series resistance through a multi- iterative technique," in Proc. IEEE 27th International Conference on VLSI Design and 13th International Conference on Embedded Systems, Jan. 2014, pp. 427–432.
7. A. Kumari and S. Kumar, "Impact of some important parameters on the drain current and threshold voltage of nanoscale strained-Si MOSFETs," in Proc. National Conference on Electronics, Communication and Signal Processing, Sept. 2013, pp. 38–43.
8. P. Vaishnav, A. Kumari, and T. Kumar, "Integrated 32nm technology," in Proc. National Conference on "VLSI Embedded Systems, Signal Processing and Communication Technologies", Mar. 2010, pp. 16-17.
9. A. Kumari and P. Vaishnav, "Effect of 32nm scale," in 2010 National Conference "Technologia'10", Feb. 2010.

Poster Presented:

1. J. Saha, A. Kumari, S. Jha, and S. Kumar, "On the voltage transfer characteristics (VTC) of some nanoscale metal-oxide-semiconductor field-effect-transistors (MOSFETs)," in Physics of Semiconductor Devices, V.K. Jain and A. Verma, Eds. New York, NY, USA: Springer-Verlag, 2014, pp. 211–214.

Workshops/Expert Talks attended:

- "Robust Nanoscale Circuit Design in Strain Enabled Technology (SET-2014)," organized by Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, India, 11th Sep. 2014.
- 5th International Workshop on Reliability Aware System Design and Test, organized by IIT Bombay, Mumbai, India, 5-10 Jan. 2014.
- 17th International Workshop on The Physics of Semiconductor Devices, organized by Amity Institute of Advanced Research and Studies (Material & Devices), Amity University, Noida, India, 10-13 Dec. 2013.
- National Workshop on "Digital Image Processing", organized by Department of Electronics and Communication Engineering, MP Christian College of Engineering and Technology, Bhilai, India, 5-7 Feb. 2010.

Awards and Honours:

- Co-Convener, International Conference on Fourth Industrial Revolution based Technology and Practices-2022, Quantum University, Roorkee.
- Session Chair in IEEE CISES-2023, Apr. 2023 at GLBITM Greater Noida.

Membership:

IEEE

Research Interest:

- Nanoscale strained MOSFETs and circuits.
- CMOS – based on Junctionless and Junction-based devices.
- Machine Learning
- Artificial Intelligence

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